

Oscillator (CMOS/LVPECL/LVDS/HCSL Output)

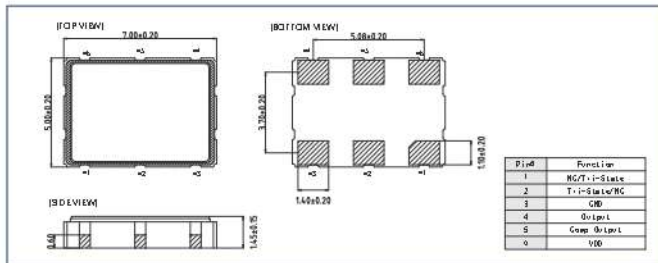
4.6 LV7050

7.0 x 5.0 mm SMD LVPECL/LVDS/HCSL Crystal Oscillator

FEATURES

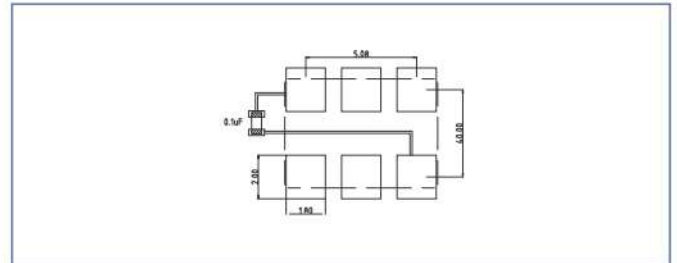
- Typical 7.0 x 5.0 x 1.45 mm hermetically sealed ceramic package
- Very low jitter performance: typical 0.3 pS RMS from 12 k ~ 20 MHz
- Fundamental/3rd overtone crystal design
- Output frequency up to 320 MHz
- Operating temperature up to 125°C
- Tri-state enable/disable

DIMENSIONS



TYPICAL APPLICATION

- 10Gbit Ethernet, Fiber Channel, Storage Area Network, SONET
- Enterprise Servers, Reference clocks for ADC and DAC
- Telecom



ELECTRICAL SPECIFICATION

Parameter		LVPECL				LVDS				Unit
		3.3V		2.5V		3.3V		2.5V		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Supply Voltage Variation (VDD)		VDD-5%	VDD+5%	VDD-5%	VDD+5%	VDD-5%	VDD+5%	VDD-5%	VDD+5%	V
Frequency Range		10	320	10	320	10	320	10	320	MHz
Standard Frequency		77.76, 106.25, 125, 155.52, 156.25, 187.5, 212.5, 312.5								
Supply Current	10MHz≤F _o <160MHz	—	75	—	75	—	50	—	50	mA
	160MHz≤F _o <250MHz	—	100	—	100	—	50	—	50	
	250MHz≤F _o <320MHz	—	100	—	100	—	65	—	65	
Output Level	Output High	2.275	—	1.475	—	—	1.6	—	1.6	V
	Output Low	—	1.68	—	0.88	0.9	—	0.9	—	
Transition Time: Rise/Fall Time+		—	1	—	1	—	1	—	1	nSec
Startup Time		—	10	—	10	—	10	—	10	mSec
Tri-State (Input to Pin2 or Pin1)	Enable (High Voltage or Floating)	2.31	—	1.75	—	2.31	—	1.75	—	V
	Disable (Low Voltage or GND)	—	0.99	—	0.75	—	0.99	—	0.75	
Aging (@25°C, 1st Year)		—	±3	—	±3	—	±3	—	±3	ppm
Storage Temp. Range		-55	125	-55	125	-55	125	-55	125	°C
Phase Noise @ 156.25 MHz	100 Hz	-100		-100		-100		-100		dBc/Hz
	1 kHz	-130		-130		-130		-130		
	10 kHz	-145		-145		-145		-145		
RMS Phase Jitter (Intergrated 12 KHz ~ 20MHz)	F _o <80MHz	—	1	—	1	—	1	—	1	pSec
	80MHz≤F _o <125MHz	—	0.5	—	0.5	—	0.5	—	0.5	
	125MHz≤F _o <170MHz	—	0.3	—	0.3	—	0.3	—	0.3	
	170MHz≤F _o <200MHz	—	0.5	—	0.5	—	0.5	—	0.5	
	200MHz≤F _o	—	0.3	—	0.3	—	0.3	—	0.3	

Oscillator (CMOS/LVPECL/LVDS/HCSL Output)

Parameter		HCSL				Unit
		3.3V		2.5V		
		Min.	Max.	Min.	Max.	
Supply Voltage Variation(VDD)		VDD-5%	VDD+5%	VDD-5%	VDD+5%	V
Frequency Range		25	175	25	175	MHz
Standard Frequency		100				
Supply Current 25MHz≤F _o ≤175MHz		—	50	—	50	mA
Output Level	Output High	0.6	—	0.58	—	V
	Output Low	—	0.15	—	0.15	
Transition Time: Rise/Fall Time+		—	0.5	—	0.5	nSec
Startup Time		—	10	—	10	mSec
Tri-State (Input to Pin2 or Pin1)	Enable (High Voltage or Floating)	0.7VDD	—	0.7VDD	—	V
	Disable (Low Voltage or GND)	—	0.3VDD	—	0.3VDD	
Aging (@25°C, 1st Year)		—	±3	—	±3	ppm
Storage Temp. Range		-55	125	-55	125	°C
RMS Phase Jitter (Intergrated 12 KHz ~ 20MHz)	25MHz≤F _o ≤175MHz	—	0.5	—	0.5	pSec

Standard frequencies are frequencies which the crystal has been designed and does not imply a stock position.

+ Transition times are measured between 20% and 80% of VDD.

FREQ. STABILITY vs. TEMP. RANGE

Temp. (°C)	ppm	±25	±50
-10 ~ +60		○	○
-20 ~ +70		○	○
-40 ~ +85		△	○
-40 ~ +125		×	○

*○: Available △: Condition ×: Not available

*Inclusive of calibration @ 25 °C, operating temperature range, input voltage variation, load variation, aging (1st year), shock, and vibration

Note: not all combination of options are available. Other specifications may be available upon request.
Specifications subject to change without notice.