Oscillator (CMOS/LVPECL/LVDS/HCSL Output)

4.8 ULV7050

7.0 x 5.0 mm SMD Ultra Low Phase Jitter LVPECL Crystal Oscillator

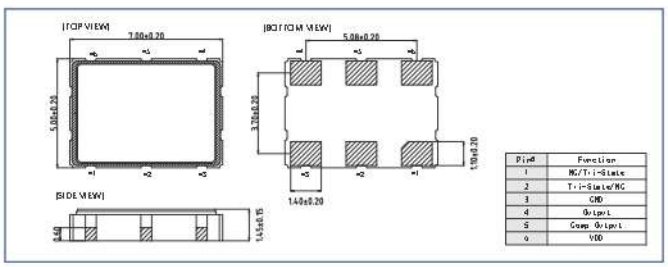
FEATURES

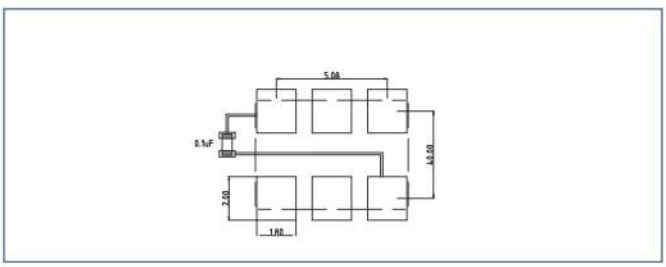
- Typical 7.0 x 5.0 x 1.45 mm 6 pads ceramic SMD package.
- Ultra low jitter performance: < 100 fs RMS from 12k ~ 20MHz
- Tight symmetry (45 to 55%) available
- Complementary output

TYPICAL APPLICATION

- 40 Gbit/100 Gbit Ethernet, MAN, SONET
- WLAN/WiMAX, xDSL
- Fiber Channel
- Test Instrumentation

DIMENSIONS





ELECTRICAL SPECIFICATION

Parameter		LVPECL				Unit
		3.3V		2.5V		
		Min.	Max.	Min.	Max.	
Supply Voltage Variation (VDD)		VDD-5%	VDD+5%	VDD-5%	VDD+5%	V
Frequency Range		70	170	100	160	MHz
Standard Frequency		100, 125, 155.52, 156.25				
Supply Current	25MHz≤F_O<175MHz	—	75	—	75	mA
Output Level	Output High	2.275	—	1.475	—	V
	Output Low	—	1.68	—	1.095	
Transition Time: Rise/Fall Time+		—	1	—	1	nSec
Startup Time		—	10	—	10	mSec
Tri-State (Input to Pin2 or Pin1)	Enable (High Voltage or Floating)	2.31	—	1.75	—	V
	Disable (Low Voltage or GND)	—	0.99	—	0.75	
Aging (@25°C, 1st Year)		—	±3	—	±3	ppm
Storage Temp. Range		-55	125	-55	125	°C
Phase Noise @ 156.25 MHz	100 Hz	-100		-100		dBc/Hz
	1 kHz	-130		-130		
	10 kHz	-150		-150		
RMS Phase Jitter (Intergrated 12 KHz ~ 20MHz)	70MHz≤F_O≤170MHz	—	0.1	—	0.1	pSec

FREQ. STABILITY vs. TEMP. RANGE

Temp.(°C) \ ppm	±25	±50
-10 ~ +60	△	○
-20 ~ +70	△	○
-40 ~ +85	×	○

*○: Available △: Condition X: Not available
*Inclusive of calibration @ 25 °C, operating temperature range, input voltage variation, load variation, aging (1st year), shock, and vibration.

Note: not all combination of options are available. Other specifications may be available upon request.
Specifications subject to change without notice.